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Design of Image Processing System Based on Charge Coupled Device

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Abstract

To speed up the image acquisition and make full use of effective information, a design method of CCD partial image scanning system is presented. The system achieves to functions of the high -speed data collection, the high -speed video data compression the real time video data Network Transmission and the real time compression picture data storage. the data processed was transferred to PC through USB2.0 real-time to reconstruct defects microscopic images. The experimental results demonstrated that defects within 50μm-1000μm were inspected effectively by the CCD scanning defects inspection instrument, that this method has a repetition error no more than 2.24 pixels, with high precision and good anti-noise ability.

Keywords*: FPGA, CCD, image acquisition, image processing*

1. Introduction

Image processing system becomes a highly integrated data processing system with high speed and accuracy. There is a increasingly high demand on the smaller size, lower power consumption, higher speed and update capabilities. Using merely DSP or ASIC to implement Image processing system has been difficult to meet these needs. A large number of proven, FPGA's parallel processing capabilities and pipelining can significantly improve image processing speed, the need to use reconfigurable FPGA-based processor to accelerate image processing applications becomes more and more important.

With the development of technology of science and the widespread application of data acquisition system, the demands of data acquisition system for the speed, accuracy, easy operation and real-time requirement have been improved [1-3]. As a new kind of PC bus interface specification, USB is widely used in data collection system for its advantages. The technology of FPGA has its own particular advantages, which has been widely used in the fields of communications, data acquisitions and image manipulation etc [3-6]. Taking full of the advantages of USB and FPGA mentioned above, the high-speed data acquisition system based on the technology of FPGA and USB2.0 was designed in this paper.

2. The Hardware Design of the Defect Processing System

One of the major features of the material detecting is the enormous data .Take the polymer film which runs quite quickly as an example. For a 1024-pixel CCD which has a scanning frequency of 1000 times/s, With a 8-bit A/D converter, if each pixel is sampled twice, then 2.048×106 Bits are sampled every second and in correspondence 20Mb processing data. Therefore, it is a major concern as how to solve the problem of massive data processing in the real-time data processing.

In detecting the image defect, it is desirable to observe the morphology of defects. Therefore, we adopt the second program to get the micro-image of the defect. As an answer to the problem of massive data processing, a defect processing system based on FPGA is designed through organically combine the high speed of FPGA and the flexibility of PC through high-speed USB. The system construe is shown in figure 1. The signal acquisition module digitalize the CCD output signal, and FPGA module which is the core module of the system,

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completes the image pre-processing including the data compression and data package, etc. The data are then sent to the host computer for follow-up processing.

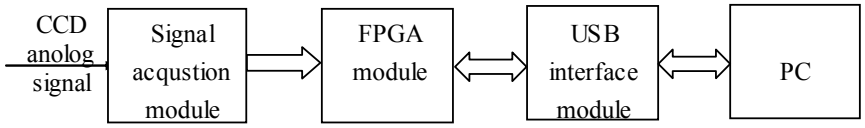

Figure 1. Defects data processing system

3. Signal Acquisition Module

The main function of the signal acquisition module is to digitalize the analog signal of the image for the CCD photographic input. The signal acquisition module is shown in figure 2. It can be seen that it is consisted of the signal conditioning circuit, A/DC circuit, power source circuit and power lever conversion circuit. The CCD output analog signal is firstly conditioned, then converted into digital signal by the A/DC circuit under the control of FPGA, which is triggered by the transferring signal SH, so comes the need to transform the power level to comply with the working condition of FPGA.

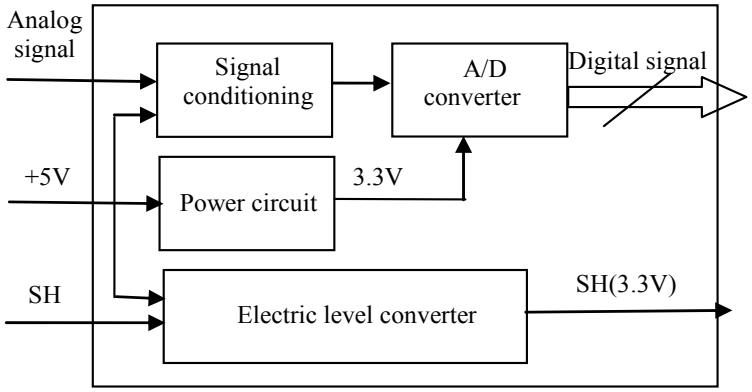

Figure 2. Signal acquisition module

FPGA module is the core part of the defect processing system, carrying all the digital circuit part. During the designing process, where the system-on-chip is emphasized, the FPGA part achieves all the required digital logic, including the adder, comparators, buffers, PLL (Phase-locked Loop, PLL), counters, MUX, USB interface logic. By doing this, we get an fully adjustable digital part, which possesses a strong adaptability and flexibility by simply updating the FPGA program in compliance with requirements.

3.1. Signal Conditioning Circuit

There needs a signal conditioning circuit before the A/DC circuit since the amplitude of the CCD analog output signal is often within 4V, while the peak voltage of the A/DC circuit is 2V. The process of conditioning includes amplifying, buffering, calibrating the signal to make it suitable for the A/DC input. Then digitalize the signal before it is sent to the micro controller and other digital devices for the follow-up data processing. The key operation lies in choosing operational amplifier.

This paper adopts the low-power voltage feedback amplifier AD8052 made by AD corporation of American. The amplifier input voltage range from -0.2V~4V, make it desirable to adjust the voltage range of the CCD output signal. The signal conditioning circuit is shown as

figure 3. Pin 8 is the working voltage, stimulated by the single power supply +5V. Signal and AD sigin are the input and output signal respectively.

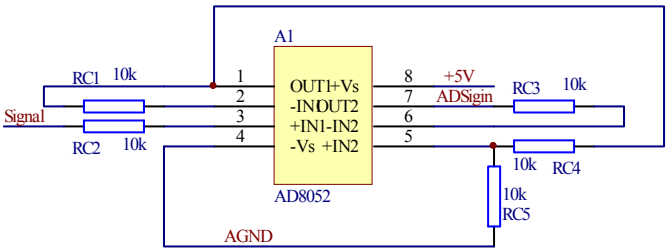

Figure 3. Conditioning circuit

3.2. A/D Conversion Circuit

The A/D conversion circuit collect the analog signal according to the pre-select sampling period. For the consideration of upgrading in the future, the design adopt the AD9203 chip which has an accuracy of 10 bit and the peak sampling frequency of 40MHz. AD9203 is a single-channel, low-voltage high-speed A/D conversion chip by the AD corporation. It has a reliable accuracy that can sustain at 10-bit precision in the whole range of sampling band with. The working voltage has a flexible range of 2.7V-3.6V, make it suitable for portable device in low-voltage, high-speed operation. The clock signal CLOCK is externally provided through the CLK pin. The AD9203 starts sampling and quantizating the amplitude when the signal hops to low level. The conversion circuit is shown as figure 4. The input analog signal and the conversion clock signal ADCLK are connected to the pin 25 and pin 15. The converted 10-bit digital signal ADD0-ADD9 are connected to pin 3~12 for the DSP in the FPGA.

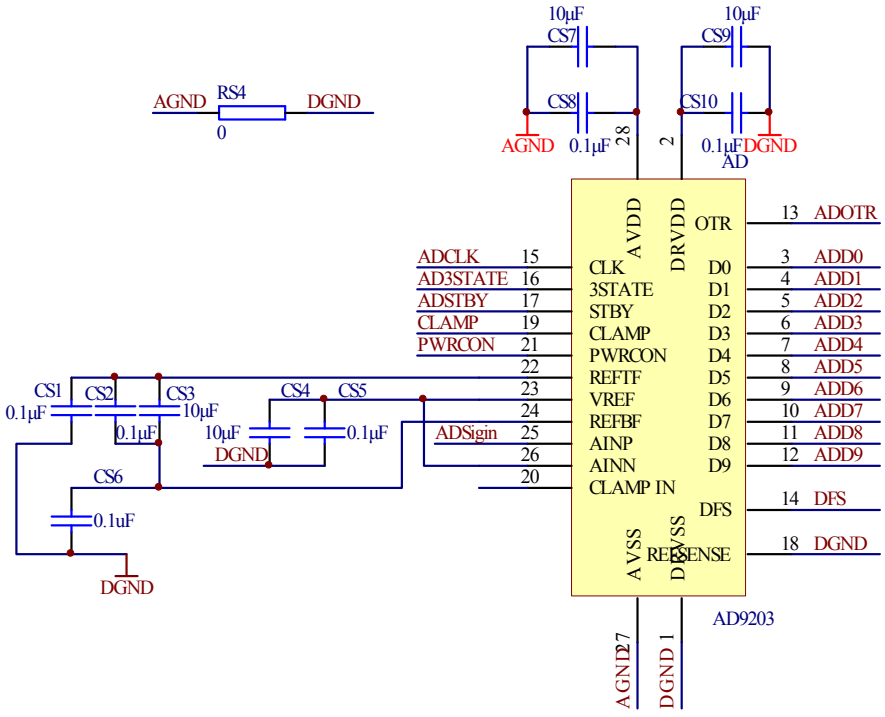

Figure 4. A/D convert circuit

3.3. Power Source Circuit

The voltage conversion circuit is designed to convert the source voltage of 5V to the A/DC chip and I/O of FPGA voltage of 3.3V. The adopted voltage conversion chip is LT1587CM-3.3 and the circuit is shown as figure 5. The inserted fuse is to protect the circuit from over flow of current .

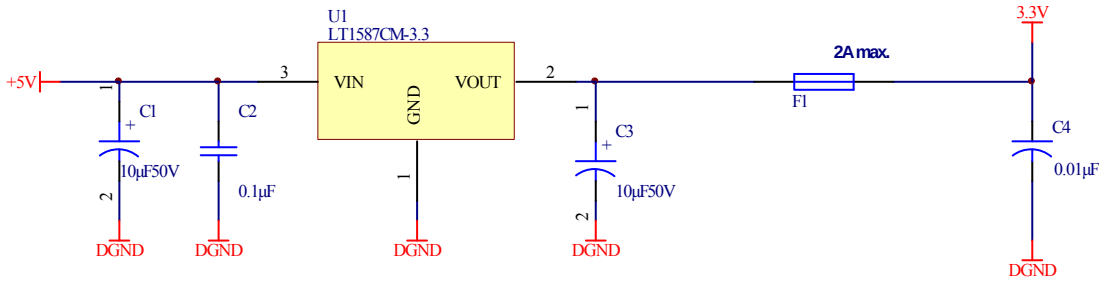

Figure 5. Voltage convert module

4. The Configuration Mode of FPGA

At present, there are a variety of configuration modes, and few manufactures share the common configuration standard. Provided by Altera are mainly the three types: AS (active serial) which is shown as figure 6; PS (passive serial)[7-9]; JTAG, which is shown as figure 7. The system adopt AS+JTAG mode. The JTAG mode is use in downloading debugging program, and the AS is applied to incur the program to the configuration chip after it is debugged correctly. The adopted EPCS4 can fully meet the designing requirements for its capacity 4 times larger than EPCS1.

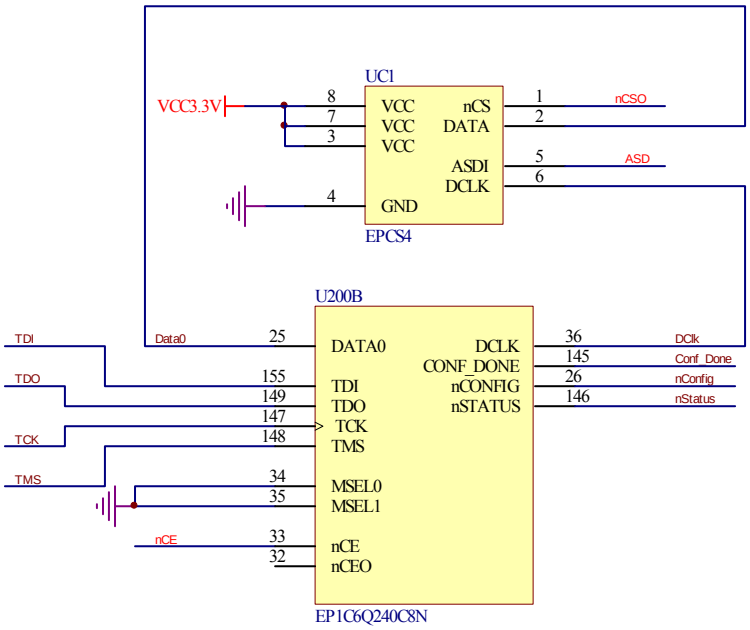

Figure 6. AS configuration mode

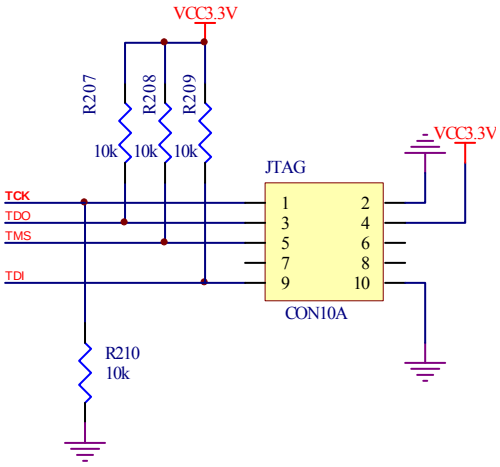

Figure 7. JTAG circuit

5. FPGA-Based Data Processing Structure

Overall block diagrams of FPGA-based data-processing structure are shown in Figure 8. SH pulse as the start signal of the clock counting unit, counter 2 provides the criterion of state switch for other modules. A/D control unit output waveform controls A/D conversion chip to convert analog signal that CCD module outputs to 10-bit digital signal. Digital signal is divided into two roads, one of which enters dynamic threshold calculation unit to calculate the threshold; the other one of which is compared with a 10-bit dynamic threshold to extract the defect data. Through the data encapsulation module, defect data generates the appropriate data structure; after passing through the FIFO buffer, defect data will be outputted under FIFO control unit's control. Some of these sub-modules are designed by Mega Wizard based on FPGA macro cell, while some are implemented through VHDL.

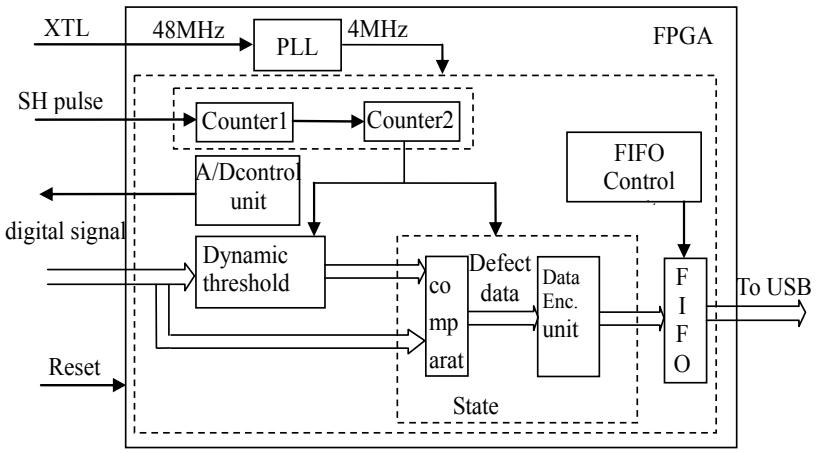

Figure 8. FPGA structure frame

6. The Simulation Result

The designing requirements for the system is to replace the traditional digital circuit chips and at the same time to complete a possible number of time temporal logic control, storage and transmission tasks. Using the macro function resources in the FPGA, we get the PLL, FIFO module; using the programmable logic resources and the self-designed VHDL code, we fulfill the function of counter, logic control and State machine, thus integrating all the digital

parts in the FPGA which used to call for several separate chips. On account of this, it is much easier to design the hardware board and the operations of controlling, predicating, verification, extending and adjusting.

Realize and simulate the above function on Quartus□6.0, and the results are shown in figure 9. The FPGA in use is the EP1C6Q240C8 of the Cyclone series by Altera Corporation. It has a logic cell utilization of 13%, pin utilization of 96% and memory cell utilization 71%.

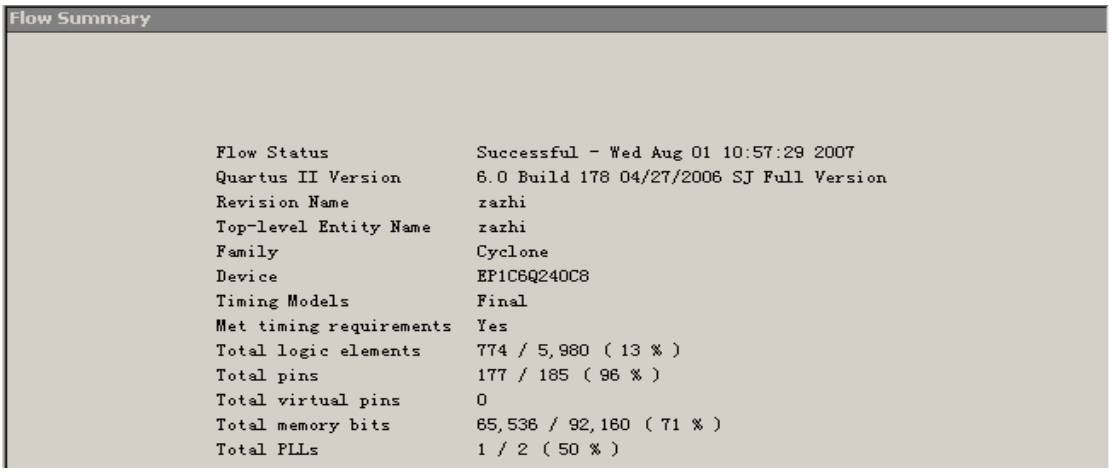

Figure 9. Compiling results

The timing simulation results of the defect are shown in figure 10. The simulation results are all hexadecimal data. ADDATA is the input data. The defects are stored in FIFO after they are detected and bite-marked. FFFF is the line flag, 8005, 8006, 8007, 8008, 8009, 800A, 800B, 800C, 800D, 800E are the value stored in FIFO of the defects 005, 006, 007, 008, 009, 00A, 00B, 00C, 00D, 00E, and 0711 is the bottom position of the defect.

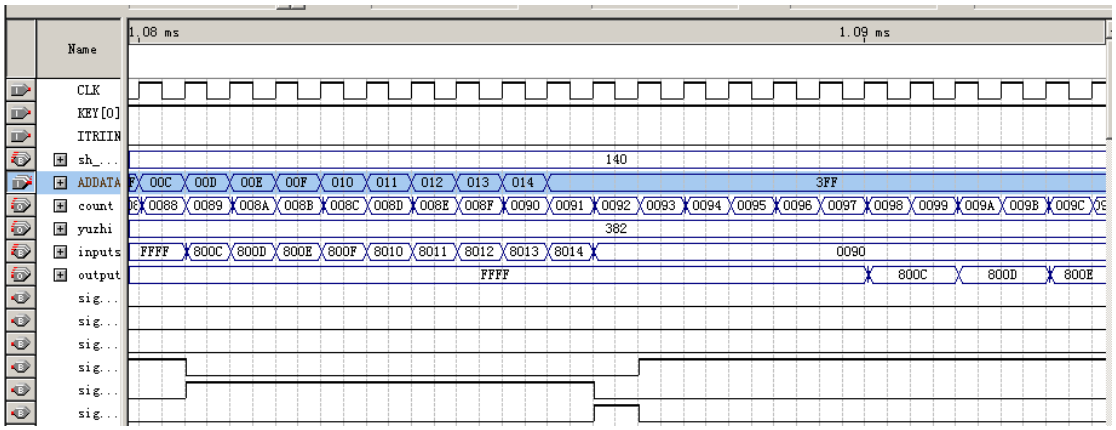

Figure 10. Simulation results

7. Experimental Verification and Analysis

To verify the effectiveness of the real-time processing of the defect based on FPGA, an experiment is carried out on the CCD scanning and detesting device to verify and analyse the standard template containing 5 defects and actual polymer film.

The experiment test 3 standard templates with defects. The obtained image of the defect by the high pixel camera is shown in figure 11. The diameters of the defect is 1000μm, 400μm, 70um respectively.

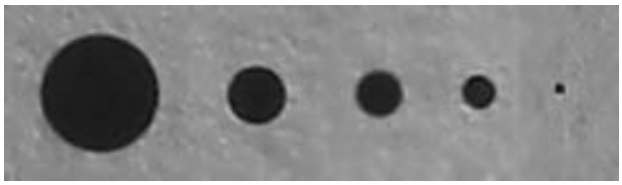

Figure 11. Standard defects images

Pass the templates through the detecting device at 20mm/s for 100 times. The experiment results show a 100% detection rate for the defect over 70 μm. The host computer can real-time show the micro-image of the defect by reconstructing the defect by the 3 size. One of the reconstructed image is shown in figure 12. The marked data include the serial number, the sampling points in accordance to the largest horizontal size and the vertical scanning times. In order to upgrade the processing speed of the system, the scanning image is compressed and reduced in quantity while still meets the requirements of shape and gray-scale information.

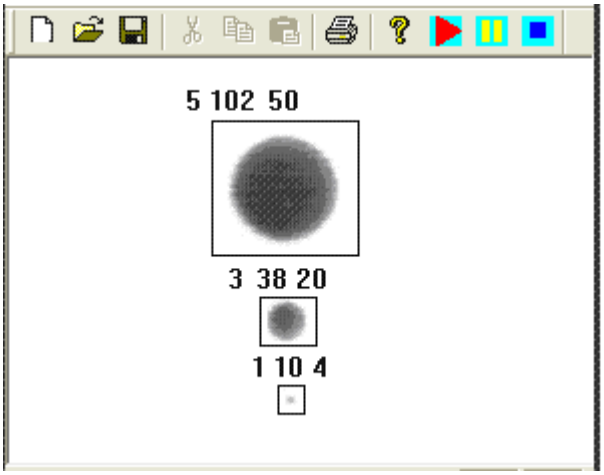

Figure 12. Reconstructed defects images

Take down the characteristics of the data. The actual horizontal size, the mean size and mean error are shown in table 1.

Table 1. Inspecting results

Actual size /μm	Measured mean size/μm	Mean error/%
1000	1009.1	0.91
400	407.3	1.83
70	77.4	10.6

The detecting result shows that the smaller the size, the larger the error. Defect of 70 μm has the biggest error, while the detesting errors of other defects are below 2.48%, which is the result of the CCD resolution and camera rate of the detection system.

8. Conclusion

In this paper, FPGA-based high-speed signal acquisition and storage systems solution for image collection and intelligent storage system design is put forward, which is characterized by low-cost, small size, low power consumption and storage convenience. In this paper, based on system design dividing system into modules, and then design each module, completing the final test.

Pre-process the image with the specific FPGA, then confine the defect by the dynamic threshold. While maintaining the whole information of the defect , we sample and package the image. By doing this, the data uploaded and the data processing are greatly reduced, thus upgrading the accuracy of the device. After testing, the system achieves the desired function, has better real-time and reliability, small volume, convenient control with a wide range of applications.

Acknowledgment

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